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ATTORNEY DOCKET NO. **10030557-1**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Reid Hayhow

Serial No.: 10/666,024 **Examiner:** Phung M. Chung

Filing Date: September 18, 2003 **Group Art Unit:** 2138

Title: METHODS AND SYSTEMS FOR DETERMINING MEMORY REQUIREMENTS FOR DEVICE TESTING

COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria VA 22313-1450

TRANSMITTAL OF APPEAL BRIEF

Sir:

Transmitted herewith is the Appeal Brief in this application with respect to the Notice of Appeal filed on March 30, 2007 .

The fee for filing this Appeal Brief is (37 CFR 1.17(c)) **$500.00**.

(complete (a) or (b) as applicable)

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136(a) apply.

☐ (a) Applicant petitions for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)(1)-(5)) for the total number of months checked below:

☐	one month	$ 120.00
☐	two months	$ 450.00
☐	three months	$1020.00
☐	four months	$1590.00

☐ The extension fee has already been filled in this application.

☒ (b) Applicant believes that no extension of term is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

Please charge to Deposit Account **08-2623** the sum of $500.00 . At any time during the pendency of this application, please charge any fees required or credit any overpayment to Deposit Account **08-2623** pursuant to 37 CFR 1.25.

A duplicate copy of this transmittal letter is enclosed.

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Date of Deposit: **OR**

☒ I hereby certify that this paper is being submitted electronically via EFS-Web to the Patent and Trademark Office on the date shown below.

Date of submission: May 30, 2007

Typed Name: Chasity C. Rossum

Signature: _____

Respectfully submitted,

Reid Hayhow

By _____

Gregory W. Osterloth
Attorney/Agent for Applicant(s)

Reg. No. 36,232

Date: May 30, 2007

Telephone No. (303) 295-8205

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Signature

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Reid Hayhow

By

Gregory W. Osterloth
Attorney/Agent for Applicant(s)

Reg. No. 36,232

Date: May 30, 2007

Telephone No. (303) 295-8205

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Appl. No.	:	10/666,024	Confirmation No. : 7952
Appellant	:	Reid Hayhow	
Filed	:	9/18/2003	
TC/A.U.	:	2138	
Examiner	:	Phung M. Chung	
Docket No.	:	10030557-1	

Mail Stop Appeal Brief – Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

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Appellant	:	Reid Hayhow	
Filed	:	9/18/2003	
TC/A.U.	:	2138	
Examiner	:	Phung M. Chung	
Docket No.	:	10030557-1	

Mail Stop Appeal Brief – Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF

Dear Sir:

This Appeal Brief is submitted in response to the Examiner's Final Office Action dated January 31, 2007.

Appellants filed a Notice of Appeal on March 30, 2007.

Real Party in Interest

The real party in interest is Verigy (Singapore) Pte. Ltd., a Singapore limited liability company.

Related Appeals and Interferences

There are no related appeals and/or interferences.

Status of Claims

Claims 1-16 are pending, all of which stand rejected.

A copy of the claims is attached as a Claims Appendix to this Appeal Brief.

Status of Amendments

No amendments were made to the claims subsequent to final rejection. All amendments have been entered.

Summary of Claimed Subject Matter

In one embodiment (claim 1), a method comprises: 1) reading a test file including a plurality of test vectors to be applied to a device (150, FIG. 1) (200, FIG. 2; p. 4, lines 1-3 of par. [0013]); and 2) determining a required memory needed to execute the plurality of test vectors (205, FIG. 2; pp. 4-5, lines 3-8 of par. [0013]).

In another embodiment (claim 10), a system comprises: 1) logic (160, FIG. 1; p. 4, lines 1-6 of par. [0012]) to read a test file including a plurality of test vectors and to determine a required memory needed to execute the plurality of test vectors (200, 205, FIG. 2; pp. 4-5, lines 1-8 of par. [0013]); and 2) a tester (100, FIG. 1), communicatively coupled to the logic, to apply the plurality of test vectors to a device (150, FIG. 1; p. 4, lines 1-5 of par. [0010] and lines 1-7 of par. [0011]).

Grounds of Rejection to be Reviewed on Appeal

1. Whether claims 1-16 should be rejected under 35 USC 102(b) as being anticipated by Regelman (US Pat. No. 6,574,626).

Argument

1. Claims 1-16 should not be rejected under 35 USC 102(b) as being anticipated by Regelman (US Pat. No. 6,574,626; hereinafter referred to as "Regelman").

Claims 1, 7-10, 14 & 15:

With respect to claim 1, the Examiner asserts that, because Regelman teaches that a "tester must be equipped with a significant amount of memory to properly store all of the test vectors that comprise a single test program", it necessarily follows that Regelman's tester must determine a required memory needed to execute the test vectors. Although Regelman does not explicitly state this, the Examiner asserts that, "This is. . .what an engineer should do to determine a required memory capacity that could properly store all of the test vectors before executing the test vectors." *See*, 1/30/2007 Final Office Action, p. 2, sec. 3. Appellant respectfully disagrees.

To begin, Regelman neither teaches nor suggests a step of "determining a required memory needed to execute [a] plurality of test vectors". Although the Examiner asserts that such a step is "inherent" in Regelman's teachings, appellant notes that there are other ways of dealing with a plurality of test vectors that exceed the storage limitations of a memory. For example, Regelman could attempt to load a plurality of test vectors into memory, and if they do not fit within the memory, a failure could be indicated, and a user could then add more memory and try once again to load the test vectors. Alternately, a user could simply purchase significantly more memory than what he believes is needed, to make sure that the storage requirements of a plurality of test vectors never exceed the size of a tester's memory.

As a result of there being other ways to deal with the problem of a plurality of test vectors exceeding the size of available memory, appellant does not believe it is "inherent" that Regelman *must* "determine" any sort of "required memory needed to execute a plurality of test vectors. This being the case, appellants assert that

Regelman does not teach the step of "determining a required memory needed to execute the plurality of test vectors", and appellant's claim 1 should be allowed over Regelman's teachings.

Claims 7-9 should be allowed, at least, because they depend from claim 1.

Claim 10 should be allowed, at least, for reasons similar to why claim 1 should be allowed.

Claims 14 & 15 should be allowed, at least, because they depend from claim 10.

Claims 2-4 & 11-13:

With respect to claims 2-4, the Examiner asserts that Regelman teaches "determining a required memory needed for each of a plurality of boards of a tester to execute the test vectors for the board" (where the Examiner deems Regelman's "Test Stations" to be equivalent to "boards"); "determining a required memory needed for each of a plurality of pins of a tester to execute the test vectors for the pin" (col. 4, lines 5-20); and "counting the number of test vectors for each test in the test file" (col. 2, lines 21-35). However, although the Examiner has attempted to correlate elements of appellant's claims with elements of Regelman's teachings, the Examiner has not shown where Regelman teaches "determining the required memory" needed for these elements to execute a plurality of test vectors. This is because Regelman contains no such teaching.

Claims 2-4 should be allowed because they depend from claim 1, and for this additional basis.

Claims 11-13 should be allowed, at least, for reasons similar to why claims 2-4 should be allowed.

Claims 5 & 6:

Claim 5 recites a very specific method for "determining a required memory needed to execute a plurality of test vectors". The method involves 1) determining a first memory requirement needed for a first pin of a tester to execute the test vectors for a first test in the test file, and then 2) setting the required memory equal to the first memory requirement. Thereafter, and for each additional pin of a tester, 1) a second memory requirement needed for the additional pin to execute the test vectors for the first test is determined, and 2) if the second memory requirement is greater than the first memory requirement, the required memory is set to the second memory requirement.

Although the Examiner asserts that Regelman's col. 19, lines 45-60, and col. 20, lines 1-27, teach the method set forth in claim 5, these excerpts contain no such teaching. Rather, these excerpts are directed to a process of loading "software units" into memory (and not test vectors). If a software unit does not fit in memory, a user is alerted to this fact. Nowhere does Regelman teach that the amount of memory required "to execute a plurality of test vectors" is determined.

Claim 5 should be allowed because it depends from claim 1, and for this additional basis.

Claim 6 should be allowed because it depends, ultimately, from claims 1 and 5.

Claim 16:

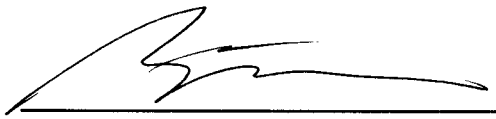
With respect to claim 16, the Examiner asserts that Regelman teaches "using the required memory to bill a customer" (col. 2, lines 30-35, and col. 7, lines 14-17). Appellant disagrees.

All that Regelman discloses is that memory is "costly". This simple observation does not teach or suggest that a customer should be billed based on a "required memory" needed to execute a plurality of test vectors.

2. Conclusion

In summary, the art of record does not teach nor suggest the subject matter of Appellant's claims 1-16. These claims are therefore believed to be allowable.

Respectfully submitted,
HOLLAND & HART, LLP

By: 

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Claims Appendix

1. A method comprising:

reading a test file including a plurality of test vectors to be applied to a device; and

determining a required memory needed to execute the plurality of test vectors.

2. The method of claim 1, wherein determining a required memory comprises determining a required memory needed for each of a plurality of boards of a tester to execute the test vectors for the board.

3. The method of claim 1, wherein determining a required memory comprises determining a required memory needed for each of a plurality of pins of a tester to execute the test vectors for the pin.

4. The method of claim 1, wherein determining a required memory comprises counting the number of test vectors for each test in the test file.

5. The method of claim 1, wherein determining a required memory comprises:

determining a first memory requirement needed for a first pin of a tester to execute the test vectors for a first test in the test file;

setting the required memory equal to the first memory requirement; and

for each additional pin of the tester,

determining a second memory requirement needed for the additional pin to execute the test vectors for the first test; and

if the second memory requirement is greater than the first memory requirement, setting the required memory equal to the second memory requirement.

6. The method of claim 5, further comprising for each additional test in the test

file:

for each pin of the tester, determining a third memory requirement for the pin to execute the test vectors for the additional test; and setting the required memory equal to the third memory requirement if the third memory requirement is greater than the required memory.

7. The method of claim 1, further comprising if the required memory exceeds an existing memory allotment, increasing the allotment of memory.

8. The method of claim 1, further comprising if the required memory exceeds an existing memory allotment, notifying a user of an amount of additional memory required.

9. The method of claim 1, wherein the device comprises a system-on-a-chip (SOC).

10. A system comprising:

logic to read a test file including a plurality of test vectors and to determine a required memory needed to execute the plurality of test vectors; and

a tester, communicatively coupled to the logic, to apply the plurality of test vectors to a device.

11. The system of claim 10, wherein the tester includes a plurality of boards, and wherein the logic is to determine a required memory needed for each board of a tester to execute the test vectors for the board.

12. The system of claim 10, wherein the tester includes a plurality of boards, each board including a plurality of pins; and wherein the logic is to determine a required memory needed for each pin to execute the test vectors for the pin.

13. The system of claim 10, wherein the logic is to determine the required memory by counting the number of test vectors for each test in the test file.

14. The system of claim 10, further comprising a user interface to notify the user of an amount of additional memory required if the required memory exceeds an existing memory allotment.

15. The system of claim 10, wherein the tester comprises a system-on-a-chip (SOC) tester.

16. The method of claim 1, further comprising using the required memory to bill a customer.

Evidence Appendix

None.

Related Proceedings Appendix

None.